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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,554	07/24/2003	Noriyuki Ito	122.1444D2	8101

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,554	ITO ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/21/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17,19,21 and 29* is/are allowed.

6)☒ Claim(s) *16,18,20 and 22-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/24/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/811,772.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 07/21/2006 regarding application 10/625,554 filed on 07/24/2003 has been entered. Amendment and remarks accompanying applicants' submission have been reviewed. Responses are provided as below. Claims 1 – 15 were cancelled. Claim 29 is newly added. Claims 16 – 29 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 29, line 4, after "wiring" insert —**graphic**—.
Claim 29, line 7, change "relevant" to —**designated**—.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 18, 20, 22 – 24 and 27 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 5,847,968 to *Miura et al.*

5. As to Claim 18, *Miura et al.* show and disclose the following subject matter:

- *Interactive editor* for use in correcting (i.e., modifying) layout and routing (i.e., placement/net wiring) in a PCB of a circuit design – [col. 3, line 19 – 37]; *Graphic display* (i.e., *editor screen*) for display placement and wiring graphic

information when packaging *design application program* is executed – [col. 14, line 29 – 33]; Notice that interactive editor displaying graphical results on an editor screen;

- *Reading out processing-related information* (e.g., *a new component*, *an area occupied by a component*, a *latest component etc*.) associated with *placement and wiring* which is stored in a *storage unit* and is designated by a *designer* (i.e., *user*) using *read-out unit* – [col. 3, line 50 – col. 4, line 16; Fig. 9];
- *Displaying* a set of menu regarding the processing-related information so readout on the editor screen by relating the processing-related information to the placement and wiring graphic information – [Fig. 9].
- Display failure...**a *designer* (i.e., a *user*) designate ... *redesign*...*placing components* by interactive edit (Step 215)** – [Fig. 9; col. 16, line 11 – 15]; *Selecting* and *determining* (i.e., *designating*) the *placement and wiring graphic information* – [col. 3, line 50 – col. 4, line 16]; Notice that (1) once the processing-related information is designated by a designer (a user) the placement and wiring graphic information associated with relevant processing-relation information is specified and to be carried out by a CAD device (2) interactive edit is performed by a designer (3) designating is performed through selection.

6. As to Claim 20, *Miura et al.* show and disclose the following subject matter:

- *Interactive editor* for use in correcting (i.e., modifying) layout and routing (i.e., placement/net wiring) in a PCB of a circuit design – [col. 3, line 19 – 37]; *Graphic display* (i.e., *editor screen*) for display *placement and wiring graphic information* (i.e., component, route and area occupied by a component et al.) when packaging *design application program* is executed – [col. 14, line 29 – 33]; Notice that interactive editor displaying graphical results on an editor screen;
- Selecting an area containing displayed placement and wiring graphic information and replacing the placement and wiring graphic information within the selected area in according with a *placement designation information* – [Fig. 17A; Fig. 17B; Fig. 17C]; Notice that (1) a dashed region in Fig. 17B

provides a placement designation information for component 3101 (2) the placement designation information in Fig. 17B designated placement distance between adjacent components and wiring illustrated by a plurality of placement and wiring graphic information.

7. As to Claim 22, *Miura et al.* show and disclose the following subject matter:

- *Interactive editor* for use in correcting (i.e., modifying) layout and routing (i.e., placement/net wiring) in a PCB of a circuit design – [col. 3, line 19 – 37]; *Graphic display* (i.e., *editor screen*) for display *placement and wiring graphic information* (i.e., component, route and area occupied by a component et al.) when packaging *design application program* is executed – [col. 14, line 29 – 33]; Notice that interactive editor displaying graphical results on an editor screen;
- Displaying *routing pattern information* (i.e., *connecting relationship information*) between components 2701 and 2707 (i.e., a plurality of pieces of placement and wiring information) – [Fig. 19 A];
- Highlighting the displayed connecting relationship information (*routing pattern information*) between *placement and wiring graphic information* of components 2701, 2702, which are selected and under study by a designer on the graphic display– [col. 13, line 13 – 21; Fig. 19B]; Notice that other placement and wiring graphic information associated with components (e.g., 2704, 2705), which are not under study, are also displayed.
- Connecting relationship information includes a wiring configuration for an arc shape line – [Fig. 19C].

8. As to Claim 23, *Miura et al.* show and disclose the following subject matter:

- *Interactive editor* for use in correcting (i.e., modifying) layout and routing (i.e., placement/net wiring) in a PCB of a circuit design – [col. 3, line 19 – 37]; *Graphic display* (i.e., *editor screen*) for display *placement and wiring graphic information* (i.e., component, route and area occupied by a component et al.) when packaging *design application program* is executed – [col. 14, line 29 – 33]; Notice that interactive editor displaying graphical results on an editor screen;

- *Displaying* in windows on an editor screen a list of names of a plurality of placement and wiring graphic information in a set of tables – [Fig. 5A – Fig. 5D];
- When one of said names (i.e., net name, component name) of said plurality of pieces of placement and wiring graphic information raised on the list is selected, displaying one of the plurality of pieces of placement and wiring graphic information so selected in accordance with a predetermined placing coordinates (i.e., position information) – [Fig. 5A – Fig. 5D]. The predetermined placing position information designates a relationship between relevant placement and wiring graphic information regarding components IC1 and IC3– [Fig. 5A; Fig. 5C].

9. As to Claim 24, *Miura et al.* show and disclose the following subject matter:

- *Interactive editor* for use in correcting (i.e., modifying) layout and routing (i.e., placement/net wiring) in a PCB of a circuit design – [col. 3, line 19 – 37]; *Graphic display* (i.e., *editor screen*) for display *placement and wiring graphic information* (i.e., component, route and area occupied by a component et al.) when packaging *design application program* is executed – [col. 14, line 29 – 33]; Notice that interactive editor displaying graphical results on an editor screen;
- Moving direction of displayed placement and wiring graphic information is preliminary designated on editor screen – [Fig. 20]; Notice that the displayed placement and wiring graphic information is moved under the moving direction on the editor screen – [Fig. 26; Fig. 27].

10. As to Claim 27, *Miura et al.* show and disclose the following subject matter:

- *Interactive editor* for use in correcting (i.e., modifying) layout and routing (i.e., placement/net wiring) in a PCB of a circuit design – [col. 3, line 19 – 37]; *Graphic display* (i.e., *editor screen*) for display a plurality of *placement and wiring graphic information* (i.e., component, route and area occupied by a component et al.) when packaging *design application program* is executed – [col. 14, line 29 – 33]; Notice that interactive editor displaying graphical results on an editor screen;

- Displaying on an editor screen an area containing a plurality of pieces of placement and wiring graphic information and displaying said area by a *frame* to which a painted-out pattern is affixed – [Fig. 17A – Fig. 17C]; It is well known in the art that, when a portion of the area within the frame is enlarged and displayed on the editor screen, a painted-out is displayed in the frame due to the fact size of the frame id fixed.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 16 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,050,091 to *Rubin* in view of U.S. Patent No. 5,847,968 to *Miura et al.*

13. As to Claims 16 and 28, *Rubin* shows and discloses the following subject matter:

- A method of controlling (net) connectivity and polygon placement of electrical circuits while modifying the design of such circuits – [col. 1, line 17 – 21; col. 2, line 1 – 21];
- *Graphic editor* (i.e., *interactive editor*) for use in *graphic design* ...displaying and manipulating both (net) connectivity and polygon geometry placement – [col. 2, line 38 – 43]; revise (i.e., modify) desired (design) records of a database – [col. 6, line 45 – 46]; When a change (i.e., modification) to a node

is requested, that change is made to a database – [col. 4, line 19 – 21]; All of the resulting changes are preserved (i.e., stored) in a database – [col. 4, line 39 – 41]; database change means 616 for updating the database 615 – [Fig. 6; col. 6, line 26 – 30]; Notice that (1) a *graphic editor* is performed by a *computer process program* to graphically modify *graphic information on placement of polygons and wiring connectivity* of a electric circuit (2) modified information is stored in a database;

- Results (i.e., modified information) are (stored in a window) and displayed to user on a *display monitor* 601 (i.e., a window display of a graphic editor) – [col. 6, line 14 – 25].

Rubin teaches displaying the modification information on a window (display monitor), he does not teach replaying the placement and wiring graphic information when associated modification information on the window is designated. But *Miura et al.* show and teach this method and other subject matter as given below:

- *Interactive editor* for use in correcting (i.e., modifying) layout and routing (i.e., placement/net wiring) in a PCB of a circuit design – [col. 3, line 19 – 37]; *Graphic display* (i.e., *editor screen*) for display *placement and wiring graphic information* (i.e., component, route and area occupied by a component et al.) when packaging *design application program* is executed – [col. 14, line 29 – 33]; Notice that interactive editor displaying graphical results on an editor screen;
- Showing a diagram containing displayed *placement and wiring graphic information* – [Fig. 17A], selecting an area and designating *placement and wiring* (i.e., modification information) within the selected area need to be modified – [Fig. 17C]; and redisplaying the placement and wiring graphic information associated to the designated modification information within the selected area on the editor screen – [Fig. 17C].

Notice that the purpose of replaying modified placement and wiring graphic information associated with a designated modification information on the window is to obtain a clear picture of the overall circuit layout for use in graphical verification of

accuracy of placement and wiring associated with the designated modification information.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Miura et al.* in replaying modified placement and wiring graphic information associated with a designated modification information on a window in order to obtain a clear picture of the overall circuit layout for use in graphical verification of accuracy of placement and wiring associated with the designated modification information.

14. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,847,968 to *Miura et al.* in view of U.S. Patent No. 5,247,455 to *Yoshikawa*.

15. As to Claim 26, *Miura et al.* show and disclose the following subject matter:

- *Interactive editor* for use in correcting (i.e., modifying) layout and routing (i.e., placement/net wiring) in a PCB of a circuit design – [col. 3, line 19 – 37]; *Graphic display* (i.e., *editor screen*) for display *placement and wiring graphic information* (i.e., component, route and area occupied by a component et al.) when packaging *design application program* (i.e., *placement and wiring processing program*) is executed – [col. 14, line 29 – 33]; Notice that interactive editor displaying graphical results on an editor screen.
- Selecting and displaying on the editor screen a plurality of pieces of placement and wiring information – [Fig. 5A – Fig. 5D]; Notice that the plurality of pieces of placement and wiring information is to be executed by the *design application program* (*placement and wiring processing program*);
- Displaying on the editor screen respective pieces of position information associated with a plurality of pieces of placement and wiring graphic information – [Fig. 5A – Fig. 5D].

Miura et al. disclose all subject matter given above, they do not teach a method of checking on positional relations between displaced respective pieces of a plurality of pieces of placement and wiring graphic information in accordance with a placement and wiring rule. But *Yoshikawa* show and teach a method of checking on positional

relationship between displayed wirings in accordance with a (placement and) wiring specification (i.e., rule) in order to avoid *design violation* caused by lattice point offset of a CAD tool thereby accurately measuring and adjusting spacings between wirings to meet design requirement – [Fig. 12; Fig. 13; Fig. 1; col. 3, line 63 – col. 4, line 12].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Yoshikawa* in checking on positional relationship between displayed wirings in accordance with a (placement and) wiring specification (i.e., rule) in order to avoid *design violation* caused by lattice point offset of a CAD tool thereby accurately measuring and adjusting spacings between wirings to meet design requirement

16. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,847,968 to *Miura et al.* in view of Power Point to *Microsoft*.

17. As to Claim 25, *Miura et al.* show and disclose the following subject matter:

- *Interactive editor* for use in correcting (i.e., modifying) layout and routing (i.e., placement/net wiring) in a PCB of a circuit design – [col. 3, line 19 – 37]; *Graphic display* (i.e., *editor screen*) for display *placement and wiring graphic information* (i.e., component, route and area occupied by a component et al.) when packaging *design application program* is executed – [col. 14, line 29 – 33]; Notice that interactive editor displaying graphical results on an editor screen.

Miura et al. teach all subject matter listed above, they do not teach designing the placement and wiring graphic information and selecting a copy command to copy the placement and wiring graphic information to a designated position on the editor screen. But, it is well known that commercial available *Power Point* software program has capabilities of graphically designing polygons and interconnect wires (i.e., placement and wiring graphic information) and grouping placement and wiring graphic information into a plurality smaller groups and/or grouping the entire placement and wiring graphic information into a bigger group. By selecting a copy command, the entire or partial of

the placement and wiring graphic information can be copied to a designated position on an editor screen.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have integrated Power Point software program in an interactive editor for providing capabilities of graphically designing polygons and interconnect wires (placement and wiring graphic information) and selecting a copy command to copy the placement and wiring graphic information to a designated position on an editor screen in order shorten development time.

Allowable Subject Matter

18. Claims 17, 19, 21 and 29 are allowed.

Claims 17, 19 and 21 are allowed due to allowable subject matter recited in the Office Action mailed 03/20/2006.

Claim 29 is allowed because that the prior art does not teach or fairly suggest the following subject matter:

- A placement/net wiring processing method using an interactive editor comprising specifying placement and wiring graphic information associated with processing-related information designed by a user on a editor screen in combination with other limitations as recited in **Claim 29**.

Response to Amendment and Remarks

19. Applicants' amendments & remarks accompany with submission of RCE filed on 07/21/2006 have been reviewed. Claim 29 is newly added. Applicants' arguments have been considered. Key arguments and responses are list as below:

[Argument 1]: Prior art (Miura et al.) neither teaches, discloses, nor suggests "said user selects and designates said process-related information displaced on said window

[Response 1]: Prior art (Miura et al.) do disclose a designer (i.e., user) designate re-implementation of package design ...placing components (i.e., processing-

related information) by interactive edit (on an edit window) – [Fig. 9; col. 16, line 11 – 15].

[Argument 2]: In prior art (Miura et al.), the placement position of each component and/or routing path is determined by the PCB CAD device not by a user.

[Response 2]: PCB CAD is an interactive computer design tool, which is implemented by a user in determination of placing position of each component on a PCB design using an edit display (window). Notice that (1) when implementing a CAD tool, it is a designer (user), who makes a selection/decision in designating a placing position (2) routing path between components is determined after positions of the components are designed by a designer (user) (3) interactive CAD tool can be implemented based on a selection chosen by a designer by using a mouse .

[Argument 3]: Prior art (Miura et al.) neither teaches, discloses, nor suggests "selecting an area containing said displayed placement and wiring graphic information on said editor screen".

[Response 3]: Prior art (Miura et al.) discloses displaying placement and wiring graphic information on a graphic display – [Fig. 17A – 17B; col. 3, line 19 – 37; col. 14, line 29 – 33].

[Argument 4]: Prior art (Rubin) neither teaches, discloses, nor suggests "redisplaying the placement and wiring graphic information associated to said designated modification information on said editor screen".

[Response 4]: But Miura et al. (Prior Art) discloses the subject matter in Fig. 17A – 17C, see details included in explanations in response to Claim 16 given above.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Sun James Lin* whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Jack Chiang* can be reached on (571) 272 - 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
August 15, 2006

SUN JAMES LIN
PRIMARY EXAMINER